Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A method comprising:

providing a first processor on a single silicon chip; loading, on the first processor, a plurality of software simulations of a corresponding plurality of second processors that ~~is~~ are to be provided in hardware on the single silicon chip;

loading, on the first processor, ~~an~~ a plurality of ~~applications~~ software applications, ~~that is~~ where one of the software applications is configured to be executed on the hardware of one of the second processors and is executed with a corresponding software simulation of the second processor on the first processor to debug the one of the software applications; and

~~executing the software simulation of the second processor and the applications software on the first processor~~setting the corresponding software simulation, that is executing the one of the software applications being debugged, to a first simulation mode, and setting at least one other software simulation that is executing a different one of the software applications, which is not being debugged, to a second simulation mode.

2. (Currently Amended) The method of claim 1:

wherein the corresponding software simulation of the corresponding second processor includes a slow, highly detailed simulation of the second processor and a fast, high-level simulation of the second processor;

and ~~further~~setting a software simulation to either the first simulation mode or the second simulation mode ~~comprising~~ comprises selecting the software simulation as either the slow, highly detailed simulation or the fast, high-level simulation.

3. (Original) The method of claim 2 wherein the slow, highly detailed simulation of the second processor includes a simulation of bus interface to the second processor and to memory and control status registers.

4. – 7. (Canceled)

8. (Currently Amended) ~~The~~ A method ~~of claim 1 further~~ comprising:

providing a first processor on a single silicon chip;

loading, on the first processor, a software simulation of a second processor that is to be provided in hardware on the single silicon chip;

loading, on the first processor, a software application to be executed on the hardware of the second processor;

executing the software simulation of the second processor and the software application on the first processor;

providing a third processor external to the single silicon chip;

wherein the software simulation of the second processor includes a first interface;

configuring the first interface to execute the software simulation of the second processor on the third processor;

loading, on the third processor, the software simulation of the second processor;

wherein the ~~applications~~ software application includes a second interface;

configuring the second interface to execute the ~~applications~~ software application on the third processor;

loading, on the third processor, the ~~applications~~ software application; and

executing the software simulation of the second processor and the ~~applications~~ software application on the third processor.

9. (Currently Amended) The method of claim 1 further comprising:

providing at least one of the second processors as hardware on the single silicon chip;

wherein each of the ~~applications~~ software applications includes an interface;

for at least one of the software applications, configuring the interface to execute the ~~applications~~ software applications on the hardware of the corresponding second processor; and

executing the ~~applications~~ software applications on the hardware of the corresponding second processor.

10. (Currently Amended) A computer program product embodied on a tangible storage medium, the program comprising executable instructions that enable the computer to:

configure a software simulation of a first processor, which is to be provided in hardware on a single silicon chip, to execute on a second processor on the single silicon chip ~~in either a slow, highly detailed simulation mode or a fast, high-level simulation mode~~; ~~and~~

configure a first ~~applications~~ software application, which is to be executed on the hardware of the first processor, to execute with the software simulation of the first processor on the second processor or to execute on the hardware of the first processor; and

set the software simulation of the first processor in either a slow, highly detailed simulation mode or a fast, high-level simulation mode based on whether the first software application is being debugged, if the first software application is configured to execute with the software simulation of the first processor.

11. (Currently Amended) The computer program product embodied on a tangible storage medium of claim 10, the program further comprising executable instructions that enable the computer to:

configure a second ~~applications~~ software application to execute on either the second processor or a processor external to the single silicon chip.

12. (Currently Amended) A method of developing software for a multi-processor chip, the method comprising:

loading, on a first processor, a plurality of software simulations of a plurality of second processors that are to be provided in hardware on a single silicon chip, each software simulation corresponding to a one of the second processors, and each software simulation ~~includes~~ including a slow, highly detailed simulation of the second processor and a fast, high-level simulation of the second processor;

selecting each software simulation as either the slow, highly detailed simulation or the fast, high-level simulation;

loading, on the first processor, a plurality of ~~applications~~ software applications, each ~~applications~~ software application to be executed on the hardware of a corresponding one of the plurality of second processors; and

executing the plurality of software simulations of the plurality of second processors and the plurality of ~~applications~~ software applications on the first processor.

13. (Original) The method of claim 12 wherein the slow, highly detailed simulation of the second processor includes a simulation of bus interface to the first processor and to memory and control status registers.

14. (Original) The method of claim 12 further comprising providing the first processor as hardware on the single silicon chip.

15. (Original) The method of claim 12 further comprising providing the first processor as hardware external to the single silicon chip.

16. (Currently Amended) The method of claim 12 further comprising:

providing a one of the plurality of second processors as hardware on the single silicon chip;

wherein each of the plurality of ~~applications~~ software applications includes an interface;

configuring the interface of the ~~applications~~ software application corresponding to the one of the plurality of the second processors to execute the ~~applications~~ software application corresponding to the one of the plurality of the second processors on the hardware of the one of the plurality of second processors; and

executing the ~~applications~~ software application on the hardware of the second processor.

17. (Currently Amended) An apparatus for developing software for a multi-processor chip comprising:

a first processor on a single silicon chip having loaded thereon,

a plurality of software simulations of a corresponding plurality of second processors that ~~is~~ are to be provided in hardware on the single silicon chip, and

~~an~~ a plurality of ~~applications~~ software applications, ~~that is~~ where one of the software application is configured to be executed on the hardware of one of the second processors and is executed with a corresponding software simulation of the second processor on the first processor to debug the one of the software applications;

wherein the first processor is configured to execute ~~the software simulation of the second processor and the applications software on the first processor~~ the software application being debugged with a software simulation set to a first simulation mode, and to execute at least one other of the software applications not being debugged with a software simulation set to a second simulation mode.

18. (Currently Amended) The apparatus of claim 17 further comprising:

a third processor external to the single silicon chip having loaded thereon the software simulation of at least one of the second processors and the corresponding ~~applications~~ software application;

the third processor configured to execute the software simulation of the second processor and the ~~applications~~ software application.

19. (New) The apparatus of claim 17

wherein each software simulation of a corresponding second processor includes a slow, highly detailed simulation of the second processor and a fast, high-level simulation of the second processor;

and the first simulation mode comprises the slow, highly detailed simulation, and the second simulation mode comprises the fast, high-level simulation.